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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,554	06/11/2001	Xinghao Chen	FIS920010060US1	5168

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 07/12/2006 have been fully considered but they are not persuasive.

The Applicant contends, "Song does not disclose performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC".

The Examiner disagrees and asserts that paragraph 1, in col. 2 on page 707 of Song teaches that PPST algorithm in Song is an extension of the PPSFP algorithm in Antreich (Antreich, K.J.; Schulz, M.H.; Accelerated Fault Simulation and Fault Grading in Combinational Circuits; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 6, Issue 5, September 1987 Page(s): 704 – 712) [hereafter referred to as Antreich]. The Examiner introduces the Antreich as a teaching reference for that which is inherent in Song. Antreich teaches that true-value simulation must be carried out for any gate or primitive in a circuit and, for each node w exiting a gate, a vector vec(w) of signal values is generated and stored (see Section III on page 705 of Antreich), that is; Antreich teaches a good machine true-value simulation on an IC with the test to obtain a vector vec(w) of values for each internal node w of the IC.

Note: the applicant admits in line 17 on page 10 of the Applicant's specification that good machine is a fault-free-circuit; hence a true-value simulation is a good machine simulation since it is a fault-free-circuit simulation.

The Applicant contends, "Song does not teach backtracing "in a single detection pass"".

The Examiner asserts that claim 1 does not recite, "backtracing "in a single detection pass"" but instead explicitly recites, "identifying potential faults to be tested by the test by backtracing, in a single detection pass".

The Examiner disagrees and asserts that Section 2 on page 707 of Song teaches that a first backtracing is performed to detect stem-critical fault values and that a second backtracing is performed from stems marked as critical is performed to gather information about the faults that were detected in the first backtracing. The Faults, however; are identified in the first backtracing, hence Song teaches identifying potential stem-critical faults to be tested by the test by a first backtracing, in a single detection pass occurring during the first backtracing.

The Applicant contends, "Song does not disclose backtracing in a single detection pass through memory elements. Song only discloses performing, the disclosed backtracing for combinational logic".

The Examiner disagrees and asserts that the backtracing in Song is for testing combinational logic in VLSI (see Introduction in Antreich). The last sentence in the second column of page 706 in Song indicates a delay in backtracing. The delay can only be attributed to memory elements required for interconnecting various combinational elements together in VLSI for the purposes of buffering, latching and synchronizing since combinational elements are substantially instantaneous in

operation. It is inconceivable that VLSI could exist as pure combinational circuitry with no sequential logic for buffering, latching and synchronizing and it is inconceivable that test patterns could be introduced into VLSI without the use sequential logic for buffering and synchronizing the test patterns and without latches for accumulating outputs from observation points in combinational logic as test patterns pass through the combinational circuitry under test in the VLSI (see Figure 8 in Maruyama, for example; Note: flip-flops and latches are memory).

The Applicant contends, "Maruyama does not try to identify faults across memories in a single detection pass".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "Maruyama does not try to identify faults across memories in a single detection pass") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim 1 recites, "identifying potential faults to be tested by the test by backtracing" by "**backtracing**, in a single detection pass, through logic,gates and memory elements" [Emphasis Added].

The Examiner asserts that according to the Applicant's own disclosure and Figure 1-8 memory for testing and **nowhere in the Applicant's specification** does the Applicant even teach identifying "faults across memories in a single detection pass". The

Examiner asserts that the claims do not recite identifying "faults across memories in a single detection pass" and furthermore there is no support in the specification for identifying "faults across memories in a single detection pass".

The Examiner disagrees with the applicant and maintains all rejections of claims 2, 6 and 8-13. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 2, 6 and 8-13 are not patentably distinct or non-obvious over the prior art of record in view of the references, Song et al. (Song, O.; Menon, P.R.; Parallel pattern fault simulation based on stem faults in combinational circuits, Proceedings International Test Conference, 10-14 Sept. 1990, Pages:706 – 711) [hereafter referred to as Song] in view of Maruyama; Daisuke (US 6205567 B1) as applied in the last office action, filed 04/10/2006. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 2, 6 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (Song, O.; Menon, P.R.; Parallel pattern fault simulation based on stem faults in combinational circuits, Proceedings International Test Conference, 10-14 Sept. 1990, Pages:706 – 711) [hereafter referred to as Song] in view of Maruyama; Daisuke (US 6205567 B1).

See the Non-Final Action filed 04/10/2006 for detailed action of prior rejections.

Conclusion

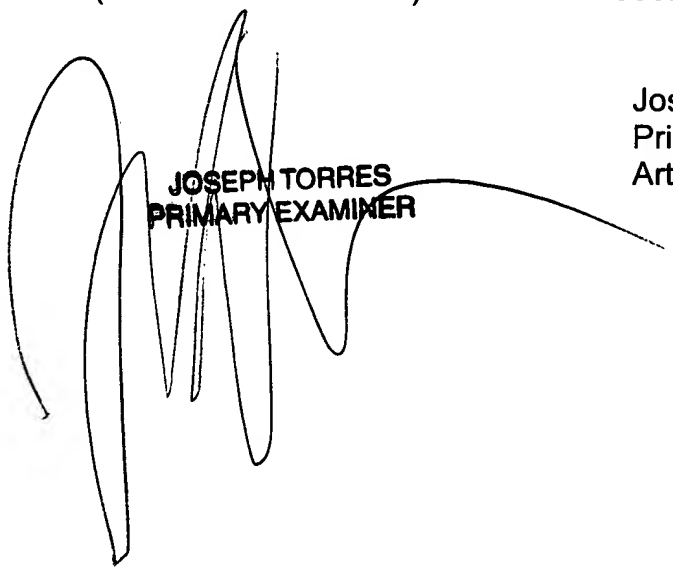
3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133